REMARKS

This communication is a full and timely response to the aforementioned Final Official Action dated March 23, 2011. By this communication, claims 1, 2 and 5-22 are cancelled, and claims 24-34 are added. Claims 3, 4 and 23 were previously cancelled. Thus, claims 24-34 are pending in the application. Claim 24 is independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Interviews

Applicants thank the Examiner for kindly conducting a telephone interview with Applicants' undersigned representative on April 28, 2011. During this interview, Applicants' representative discussed the now-cancelled claims in view of the applied references.

Applicants also thank the Examiner for kindly conducting a telephone interview with Applicants' undersigned representative and Mr. James LaBarre on June 21, 2011. During this interview, Applicants' representatives discussed disclosed embodiments of the present application as well as reasons why proposed new claims, which are renumbered as claims 23-34 above, are distinguishable over the applied references. The reasons therefor are summarized below.

II. Rejections Under 35 U.S.C. § 103

Claims 1, 12-18 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba et al. (U.S. 5,477,557, hereinafter "Inaba") in view of Kobayashi et al. (US 6,181,718, hereinafter "Kobayashi") and Nagarajan (U.S. 5,760,939). In addition, dependent claims 2, 5-11, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba and Kobayashi and Nagarajan and further in view of one or more of Takeshi et al. ("An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection." IEEE Journal of Solid-State Circuits, Volume 36, No. 12, pp 1984-

1994, December 2001, hereinafter "Takeshi"), Ito et al. (U.S. Patent No. 4,975,664, hereinafter "Ito"), and Kobayashi et al. (U.S. 5,982,793, hereinafter "Kobayashi '793).

These rejections are believed to be moot in view of the cancellation of claims 1, 2 and 5-22. These rejections are inapplicable to new claims 24-34 for at least the following reasons.

As illustrated in Figure 18 of the present application, a conventional optical semiconductor device includes an LD driving circuit 200 that drives a semiconductor laser diode (LD) 310. The LD driving circuit 200 includes a first transistor 202 which receives an antiphase signal, and a second transistor 203 which receives a positive phase signal, which is complementary to the antiphase signal. A collector of the second transistor 203 is connected to the cathode of the LD 310, while the anode of the LD 310 is connected to ground. As shown in Figure 18, there is no input from the transistors 202, 203 applied to the anode of the LD 310 (see line 17 on page 1 to line 9 on page 2 of the original specification).

Due to this arrangement, as illustrated in Figure 19, the rise time Tr and the fall time Tf of the signal applied to the LD 310 are asymmetrical. In particular, as shown in Figure 19, the fall time Tf is longer than the rise time Tr by about 40% (see lines 10-20 on page 2 of the original specification). Due to this asymmetry, the optical output waveform of the LD 310 is conspicuously deteriorated as shown in Figure 20. For instance, as shown by circle W2 in Figure 20, interference is created near an eye mask region due to the asymmetrical rise Tr and fall Tf times of the signal applied to the LD 310 (see line 21 on page 2 to line 9 on page 4 of the original specification). Consequently, the optical output waveform of the LD 310 is deteriorated due to the asymmetry between the rise Tr and fall Tf times of the output waveform for the LD driving circuit 200.

With reference to Figure 1, for example, exemplary embodiments of the present disclosure provide an optical semiconductor device which solve the above-described problem associated with conventional optical semiconductor devices, such as that of Inaba. As shown in Figure 1, the optical semiconductor device includes a first transistor 12 connected to a first resistor 15, and a second transistor 13 connected to a second resistor 16. The optical semiconductor device also includes an optical semiconductor element 20 having an anode and a cathode. In addition,

the optical semiconductor device includes a first conductor line having a first end and a second end, and a second conductor line having a third end and a fourth end. In the example of Figure 1, the first conductor line is the upper conductor line whose first end is connected between the first transistor 12 and the first resistor 15, and whose second end is connected to the anode of the optical semiconductor element. In the example of Figure 1, the second conductor line is the lower conductor line whose third end is connected between the second transistor 13 and the second resistor 16, and whose fourth end is connected to the cathode of the optical semiconductor element 20.

As illustrated in the example of Figure 1, one of the conductor lines is configured to receive a positive-phase signal as an input signal, and the other one of the conductor lines is configured to receive an antiphase signal as an input signal. Accordingly, the disclosed optical semiconductor device provides that a differential signal is applied across the anode and cathode of the optical semiconductor element 20, which results in a push-pull operation of the optical semiconductor element 20. For instance, as described in the paragraph beginning at line 19 on page 22 of the original specification, due to the above-described arrangement of the optical semiconductor device, the positive phase signal and the antiphase signal are applied to mutually opposite ends of the optical semiconductor element 20. For example, the positive phase signal is applied to the anode of the optical semiconductor element 20, while the antiphase signal is applied to the cathode of the optical semiconductor element 20, or vice versa. By this arrangement, the rise and fall times of the transistors 12, 13 are averaged, resulting in symmetric operation characteristics (see, for example, lines 13-21 on page 23 of the original specification). In contrast, in the conventional optical semiconductor device illustrated in Figure 18, when the second transistor rises 203, current flows in the LD 310, but when the second transistor 203 falls, no current flows in the LD 310. This is the reason for the asymmetrical rise and fall times discussed above which cause the deterioration in the output waveform of the LD 310 (see lines 4-12 on page 23 of the original specification).

Accordingly, the exemplary optical semiconductor element 20 illustrated in Figure 1 is push-pull driven by the differential signal applied across the optical

semiconductor element 20 through the arrangement of the first and second transistors 12, 13, the first and second resistors 15, 16 and the first and second conductor lines. The first and second resistors 15, 16 cause the positive-phase and antiphase signals respectively output from the first and second transistors 12, 13 to be applied across the optical semiconductor element 20.

Independent claim 24 recites various features of the above-described exemplary embodiment. In particular, claim 24 recites an optical semiconductor device which includes a first transistor connected to a first resistor, a second transistor connected to a second resistor, and an optical semiconductor element having an anode and a cathode. The optical semiconductor device of claim 24 also includes a first conductor line having a first end and a second end, where the first end is connected between the first transistor and the first resistor, and the second end is connected to the anode of the optical semiconductor element. In addition, claim 24 recites that the optical semiconductor device includes a second conductor line having a third end and a fourth end, where the third end is connected between the second transistor and the second resistor, and the fourth end is connected to the cathode of the optical semiconductor element. Claim 24 also recites that one of the first and second conductor lines is configured to receive a positive-phase signal as an input signal, and the other one of the first and second conductor lines is configured to receive an antiphase signal as an input signal.

With reference to Figure 2, Inaba discloses a laser drive circuit in which the collector of transistor Q1 is connected to the cathode of laser diode (LD). The collector of transistor Q2 is connected to ground, which is a constant potential. Consequently, any signal appearing at the collector of transistor Q2 will be dissipated across the resistor between the collector of transistor Q2 and ground. Inaba does not disclose or suggest a conductor line whose first end is connected between the collector of transistor Q2 and the resistor, and whose second end is connected is connected to the anode of LD. As such, the signal at the collector of transistor Q2 is not conducted to the anode of LD. Rather, Inaba discloses that the conductor of transistor Q2 is connected to ground, and hence it will be maintained at a constant potential. Therefore, in contrast to the claimed invention, Inaba does not

disclose or suggest that a differential signal from transistors Q1 and Q2 is applied across the anode and cathode of the LD.

Consequently, the LD of Inaba is not operated by a push-pull operation, and would suffer from the same deterioration in its output optical waveform as discussed above with respect to the conventional optical semiconductor device illustrated in Figure 18 of the present application, due to the asymmetry between the rise and fall times of the signal applied from the collector of transistor Q1.

Accordingly, in contrast to claim 24, Inaba does not disclose or suggest the arrangement of the first and second conductor lines which are respectively connected to the anode and cathode of the optical semiconductor element, where one of the first and second conductor lines is configured to receive a positive-phase signal as an input signal, and the other one of the first and second conductor lines is configured to receive an antiphase signal as an input signal.

In addition, Inaba does not disclose or suggest the arrangement of the first transistor, first resistor and first conductor line, where the first end of the first conductor line is connected between the first transistor and the first resistor, and the second end of the first conductor line is connected to the anode of the optical semiconductor element, as recited in claim 24. Furthermore, Inaba does not disclose or suggest the arrangement of the second transistor, second resistor and second conductor line as recited in claim 24, where the third end of the second conductor line is connected between the second transistor and the second resistor, and the fourth end of the second conductor line is connected to the cathode of the optical semiconductor element.

Similarly, Kobayashi, Nagarajan, Takeshi, Ito and Kobayashi '793 also each fail to disclose or suggest the arrangement of the first and second transistors, first and second resistors, and first and second conductor lines, as recited in claim 24.

Therefore, Applicants respectfully submit that claim 24 is patentable over Inaba, Kobayashi, Nagarajan, Takeshi, Ito and Kobayashi '793, since these references, either individually or in combination, do not disclose or suggest all the recited features of claim 24.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claim 24 is patentable over Inaba, Kobayashi, Nagarajan, Takeshi, Ito and Kobayashi '793.

New dependent claims 25-34 recite further distinguishing features over the applied references, and are also patentable by virtue of depending from claim 24. The foregoing explanation of the patentability of claim 24 is sufficiently clear such that it is believed to be unnecessary to separately demonstrate the additional patentable features of the dependent claims at this time. However, Applicants reserve the right to do should it become appropriate.

III. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this Amendment, the Examiner believes there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: June 23, 2011 By: /Jonathan R. Bowser/
Jonathan R. Bowser
Registration No. 54,574

Customer No. 21839
703 836 6620